	L #	Hits	Search Text	DBs
1	L1	154	(((instruction prefetch$3 fetch$3) near5 (queue buffer)) near50 branch) near99 (((instruction prefetch$3 fetch$3) near5 (queue buffer)) near20 (select$3 multiplex$3))	USPAT; US-PGPUB
2	L5	14903	((instruction prefetch$3 fetch$3) near5 (queue buffer))	USPAT; US-PGPUB
3	L7	1000	5 near30 (branch near20 (predict$3 history information indicat$3 target taken))	USPAT; US-PGPUB
4	L8	2889	5 near30 cache	USPAT; US-PGPUB
5	L13	11452	((instruction prefetch$3 fetch$3) near3 (queue buffer))	USPAT; US-PGPUB
6	L14	983	5 near30 (branch near10 (predict$3 history information indicat$3 target taken))	USPAT; US-PGPUB
7	L15	874	13 near30 (branch near10 (predict$3 history information indicat$3 target taken))	USPAT; US-PGPUB
8	L16	2448	13 near20 cache	USPAT; US-PGPUB
9	L18	287	15 near99 16	USPAT; US-PGPUB
10	L20	125	18 and (branch.ab,ti.)	USPAT; US-PGPUB
11	L28	278	27 and 8	USPAT; US-PGPUB
12	L34	153	28 not 20	USPAT; US-PGPUB
13	L27	428	7 and branch.ti,ab.	USPAT; US-PGPUB

	Document ID	U	Title	Current OR
1	US 20030226003 A1	☐	Information processor having delayed branch function	712/238
2	US 20030182539 A1	☐	Storing execution results of mispredicted paths in a superscalar computer processor	712/225
3	US 20030131212 A1	☐	Absolute address bits kept in branch history table	711/203
4	US 20030070062 A1	☐	System and method for reducing computing system latencies associated with branch instructions	712/234
5	US 20030028758 A1	☐	SINGLE ARRAY BANKED BRANCH TARGET BUFFER	712/238
6	US 20030005263 A1	☐	Shared resource queue for simultaneous multithreaded processing	712/218
7	US 20020194461 A1	☐	Speculative branch target address cache	712/238
8	US 20020108029 A1	☐	Program counter (PC) relative addressing mode with fast displacement	712/234
9	US 20020099926 A1	☐	Method and system for prefetching instructions in a superscalar processor	712/207
10	US 20020095566 A1	☐	METHOD FOR PROCESSING BRANCH OPERATIONS	712/239
11	US 20100054137 A1	☐	CIRCUIT ARRANGEMENT AND METHOD WITH IMPROVED BRANCH PREFETCHING FOR SHORT BRANCH INSTRUCTIONS	712/11
12	US 20100037444 A1	☐	INSTRUCTION BUFFERING MECHANISM	712/207
13	US 20100027515 A1	☐	Apparatus and method of controlling instruction fetch	712/207
14	US 6678820 B1	☐	Processor and method for separately predicting conditional branches dependent on lock acquisition	712/239
15	US 6658558 B1	☐	Branch prediction circuit selector with instruction context related condition type determining	712/239
16	US 6651162 B1	☐	Recursively accessing a branch target address cache using a target address previously accessed from the branch target address cache	712/238
17	US 6647467 B1	☐	Method and apparatus for high performance branching in pipelined microsystems	711/140
18	US 6622236 B1	☐	Microprocessor instruction fetch unit for processing instruction groups having multiple branch instructions	712/206
19	US 6611910 B2	☐	Method for processing branch operations	712/237

	Document ID	U	Title	Current OR
20	US 6609194 B1	☐	Apparatus for performing branch target address calculation based on branch type	712/238
21	US 6604191 B1	☐	Method and apparatus for accelerating instruction fetching for a processor	712/207
22	US 6598153 B1	☐	Processor and method that accelerate evaluation of pairs of condition-setting and branch instructions	712/234
23	US 6523110 B1	☐	Decoupled fetch-execute engine with static branch prediction support	712/239
24	US 6477640 B1	☐	Apparatus and method for predicting multiple branches and performing out-of-order branch resolution	712/238
25	US 6477639 B1	☐	Branch instruction mechanism for processor	712/237
26	US 6457117 B1	☐	Processor configured to predecode relative control transfer instructions and replace displacements therein with a target address	712/213
27	US 6446197 B1	☐	Two modes for executing branch instructions of different lengths and use of branch control instruction and register set loaded with target instructions	712/237
28	US 6442681 B1	☐	Pipelined central processor managing the execution of instructions with proximate successive branches in a cache-based data processing system while performing block mode transfer predictions	712/238
29	US 6427192 B1	☐	Method and apparatus for caching victimized branch predictions	711/133
30	US 6425075 B1	☐	Branch prediction device with two levels of branch prediction cache	712/239
31	US 6418525 B1	☐	Method and apparatus for reducing latency in set-associative caches using set prediction	711/213
32	US 6389531 B1	☐	Indexing branch target instruction memory using target address generated by branch control instruction to reduce branch latency	712/237
33	US 6385719 B1	☐	Method and apparatus for synchronizing parallel pipelines in a superscalar microprocessor	712/235
34	US 6374348 B1	☐	Prioritized pre-fetch/preload mechanism for loading and speculative preloading of candidate branch target instruction	712/237
35	US 6356997 B1	☐	Emulating branch instruction of different instruction set in a mixed instruction stream in a dual mode system	712/237
36	US 6324643 B1	☐	Branch prediction and target instruction control for processor	712/237
37	US 6321380 B1	☐	Method and apparatus for modifying instruction operations in a processor	717/168
38	US 6311261 B1	☐	Apparatus and method for improving superscalar processors	712/23
39	US 6304962 B1	☐	Method and apparatus for prefetching superblocks in a computer processing system	712/240
40	US 6289442 B1	☐	Circuit and method for tagging and invalidating speculatively executed instructions	712/239
41	US 6282663 B1	☐	Method and apparatus for performing power management by suppressing the speculative execution of instructions within a pipelined microprocessor	713/320

	Document ID	U	Title	Current OR
42	US 6266752 B1	☐	Reverse TLB for providing branch target address in a microprocessor having a physically-tagged cache	711/200
43	US 6253316 B1	☐	Three state branch history using one bit in a branch prediction mechanism	712/239
44	US 6250821 B1	☐	Method and apparatus for processing branch instructions in an instruction buffer	712/238
45	US 6175897 B1	☐	Synchronization of branch cache searches and allocation/modification/deletion of branch cache	711/119
46	US 6170054 B1	☐	Method and apparatus for predicting target addresses for return from subroutine instructions utilizing a return address cache	712/242
47	US 5675706 A	☐	Replacing displacement in control transfer instruction with encoding indicative of target address, including offset and target cache line location	712/213
48	US 5579798 A	☐	Method for performing branch prediction and resolution of two or more branch instructions within two or more branch prediction buffers	712/238
49	US 5579788 A	☐	Method and apparatus for high performance branching in pipelined microsystems	711/140
50	US 5346449 A	☐	Control transfer indication in predecode which identifies control transfer instruction and an alternate feature of an instruction	712/204
51	US 5119222 A	☐	Combined branch prediction and cache prefetch in a microprocessor	712/238
52	US 5119220 A	☐	Method of and apparatus for supplying multiple instruction strings whose addresses are discontinued by branch instructions	712/235
53	US 6079005 A	☐	Microprocessor including virtual address branch prediction and current page register to provide page portion of virtual and physical fetch address	711/213
54	US 6079003 A	☐	Reverse TLB for providing branch target address in a microprocessor having a physically-tagged cache	711/200
55	US 6076146 A	☐	Cache holding register for delayed update of a cache line into an instruction cache	711/125
56	US 6067616 A	☐	Branch prediction device with two levels of branch prediction cache	712/239
57	US 6061786 A	☐	Processor configured to select a next fetch address by partially decoding a byte of a control transfer instruction	712/237
58	US 6035387 A	☐	System for packing variable length instructions into fixed length blocks with indications of instruction beginning, ending, and offset within block	712/210
59	US 5996071 A	☐	Detecting self-modifying code in a pipelined processor with branch processing by comparing latched store address to subsequent target address	712/238
60	US 5983321 A	☐	Cache holding register for receiving instruction packets and for providing the instruction packets to a predecode unit and instruction cache	711/125
61	US 5964868 A	☐	Method and apparatus for implementing a speculative return stack buffer	712/234
62	US 5948100 A	☐	Branch prediction and fetch mechanism for variable length instruction, superscalar pipelined processor	712/238
63	US 5944817 A	☐	Method and apparatus for implementing a set-associative branch target buffer	712/240
64	US 5920713 A	☐	Instruction decoder including two-way emulation code branching	712/236

	Document ID	U	Title	Current OR
65	US 5918046 A	☐	Method and apparatus for a branch instruction pointer table	712/239
66	US 5918044 A	☐	Apparatus and method for instruction fetching using a multi-port instruction cache directory	712/235
67	US 5903751 A	☐	Method and apparatus for implementing a branch target buffer in CISC processor	712/238
68	US 5889986 A	☐	Instruction fetch unit including instruction buffer and secondary or branch target buffer that transfers prefetched instructions to the instruction buffer	712/237
69	US 5867698 A	☐	Apparatus and method for accessing a branch target buffer	712/238
70	US 5867683 A	☐	Method of operating a high performance superscalar microprocessor including a common reorder buffer and common register file for both integer and floating point operations	712/218
71	US 5867682 A	☐	High performance superscalar microprocessor including a circuit for converting CISC instructions to RISC operations	712/210
72	US 5570489 A	☐	Floating point stack and exchange instruction	712/222
73	US 5850543 A	☐	Microprocessor with speculative instruction pipelining storing a speculative register value within branch target buffer for use in speculatively executing instructions after a return	712/238
74	US 5842008 A	☐	Method and apparatus for implementing a branch target buffer cache with multiple BTB banks	712/240
75	US 5812839 A	☐	Dual prediction branch system having two step of branch recovery process which activated only when mispredicted branch is the oldest instruction in the out-of-order unit	712/239
76	US 5805878 A	☐	Method and apparatus for generating branch predictions for multiple branch instructions indexed by a single instruction pointer	712/239
77	US 5805853 A	☐	Superscalar microprocessor including flag operand renaming and forwarding apparatus	712/218
78	US 5802602 A	☐	Method and apparatus for performing reads of related data from a set-associative cache memory	711/204
79	US 5796998 A	☐	Apparatus and method for performing branch target address calculation and branch prediciton in parallel in an information handling system	712/239
80	US 5774710 A	☐	Cache line branch prediction scheme that shares among sets of a set associative cache	712/238
81	US 5774685 A	☐	Method and apparatus for biasing cache LRU for prefetched instructions/data based upon evaluation of speculative conditions	712/205
82	US 5751981 A	☐	High performance superscalar microprocessor including a speculative instruction queue for byte-aligning CISC instructions stored in a variable byte-length format	712/204
83	US 5748976 A	☐	Mechanism for maintaining data coherency in a branch history instruction cache	712/240
84	US 5748932 A	☐	Cache memory system for dynamically altering single cache memory line as either branch target entry or prefetch instruction queue based upon instruction sequence	715/526
85	US 5740417 A	☐	Pipelined processor operating in different power mode based on branch prediction state of branch history bit encoded as taken weakly not taken and strongly not taken states	712/239
86	US 5740415 A	☐	Instruction supplying apparatus with a branch target buffer having the contents so updated as to enhance branch prediction accuracy	712/238

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87	US 57377 50 A	☐	Partitioned single array cache memory having first and second storage regions for storing non-branch and branch instructions	711/129
88	US 57375 90 A	☐	Branch prediction system using limited branch target buffer updates	712/238
89	US 57348 81 A	☐	Detecting short branches in a prefetch buffer using target location information in a branch target cache	712/238
90	US 57322 35 A	☐	Method and system for minimizing the number of cycles required to execute semantic routines	712/209
91	US 57154 40 A	☐	Branch instruction executing device for tracing branch instruments based on instruction type	712/233
92	US 57064 92 A	☐	Method and apparatus for implementing a set-associative branch target buffer	712/238
93	US 57014 48 A	☐	Detecting segment limit violations for branch target when the branch unit does not supply the linear address	712/233
94	US 56969 58 A	☐	Method and apparatus for reducing delays following the execution of a branch instruction in an instruction pipeline	712/235
95	US 56969 55 A	☐	Floating point stack and exchange instruction	712/222
96	US 56871 10 A	☐	Array having an update circuit for updating a storage location with a value stored in another storage location	365/154
97	US 56641 36 A	☐	High performance superscalar microprocessor including a dual-pathway circuit for converting cisc instructions to risc operations	712/208
98	US 56550 98 A	☐	High performance superscalar microprocessor including a circuit for byte-aligning cisc instructions stored in a variable byte-length format	712/210
99	US 56550 97 A	☐	High performance superscalar microprocessor including an instruction cache circuit for byte-aligning CISC instructions stored in a variable byte-length format	712/204
100	US 56511 25 A	☐	High performance superscalar microprocessor including a common reorder buffer and common register file for both integer and floating point operations	712/218
101	US 56491 37 A	☐	Method and apparatus for store-into-instruction-stream detection and maintaining branch prediction cache consistency	712/207
102	US 56447 44 A	☐	Superscaler instruction pipeline having boundary identification logic for variable length instructions	712/207
103	US 56425 00 A	☐	Method and apparatus for controlling instruction in pipeline processor	712/233
104	US 56405 26 A	☐	Superscaler instruction pipeline having boundary indentification logic for variable length instructions	712/207
105	US 56320 23 A	☐	Superscalar microprocessor including flag operand renaming and forwarding apparatus	712/218
106	US 56257 89 A	☐	Apparatus for source operand dependendency analyses register renaming and rapid pipeline recovery in a microprocessor that issues and executes multiple instructions out-of-order in a single cycle	712/217
107	US 56257 87 A	☐	Superscalar instruction pipeline using alignment logic responsive to boundary identification logic for aligning and appending variable length instructions to instructions stored in cache	712/204
108	US 56236 15 A	☐	Circuit and method for reducing prefetch cycles on microprocessors	712/238

	Document ID	U	Title	Current OR
109	US 5623614 A	☐	Branch prediction cache with multiple entries for returns having multiple callers	712/240
110	US 5606675 A	☐	Data processor for invalidating prefetched instruction or branch history information	712/237
111	US 5574937 A	☐	Method and apparatus for improving instruction tracing operations in a computer system	712/23
112	US 5574871 A	☐	Method and apparatus for implementing a set-associative branch target buffer	712/200
113	US 5515518 A	☐	Two-level branch prediction cache	712/239
114	US 5511175 A	☐	Method an apparatus for store-into-instruction-stream detection and maintaining branch prediction cache consistency	712/216
115	US 5509130 A	☐	Method and apparatus for grouping multiple instructions, issuing grouped instructions simultaneously, and executing grouped instructions in a pipelined processor	712/215
116	US 5454087 A	☐	Branching system for return from subroutine using target address in return buffer accessed based on branch type information in BHT	712/240
117	US 5414822 A	☐	Method and apparatus for branch prediction using branch prediction table with improved branch prediction effectiveness	712/240
118	US 5287467 A	☐	Pipeline for removing and concurrently executing two or more branch instructions in synchronization with other instructions executing in the execution unit	712/235
119	US 5230068 A	☐	Cache memory system for dynamically altering single cache memory line as either branch target entry or pre-fetch instruction queue based upon instruction sequence	711/137
120	US 5226130 A	☐	Method and apparatus for store-into-instruction-stream detection and maintaining branch prediction cache consistency	712/238
121	US 5136696 A	☐	High-performance pipelined central processor for predicting the occurrence of executing single-cycle instructions and multicycle instructions	712/240
122	US 5050068 A	☐	Method and apparatus for using extracted program flow information to prepare for execution multiple instruction streams	712/206
123	US 4943908 A	☐	Multiple branch analyzer for prefetching cache lines	712/240
124	US 4926323 A	☐	Streamlined instruction processor	712/238
125	US 4847753 A	☐	Pipelined computer	712/238

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1	US 20040 01568 3 A1	☐	Two dimensional branch history table prefetching mechanism	712/240
2	US 20040 00321 6 A1	☐	Branch prediction apparatus and method	712/237
3	US 20030 13572 2 A1	☐	Speculative load instructions with retry	712/235
4	US 20030 09754 9 A1	☐	Predicted return address selection upon matching target in branch history table with entries in return address stack	712/240
5	US 20030 03350 5 A1	☐	Apparatus for processing instructions in a computing system	712/215
6	US 20030 01868 5 A1	☐	Method and system to perform a thread switching operation within a multithreaded processor based on detection of a branch instruction	718/102
7	US 20020 19909 2 A1	☐	Split history tables for branch prediction	712/240
8	US 20020 19446 4 A1	☐	Speculative branch target address cache with selective override by seconday predictor based on branch instruction type	712/239
9	US 20020 19446 3 A1	☐	Speculative hybrid branch direction predictor	712/239
10	US 20020 19446 2 A1	☐	Apparatus and method for selecting one of multiple target addresses stored in a speculative branch target address cache per instruction cache line	712/238
11	US 20020 19446 0 A1	☐	Apparatus, system and method for detecting and correcting erroneous speculative branch target address cache branches	712/238
12	US 20020 18883 4 A1	☐	Apparatus and method for target address replacement in speculative branch target address cache	712/238
13	US 20020 18883 3 A1	☐	Dual call/return stack branch prediction system	712/236
14	US 20020 16198 7 A1	☐	System and method including distributed instruction buffers holding a second instruction form	712/205
15	US 20020 09191 3 A1	☐	Re-order buffer managing method and processor	712/218
16	US 20020 08331 0 A1	☐	METHOD AND APPARATUS FOR PREDICTING LOOP EXIT BRANCHES	712/233
17	US 20010 03744 7 A1	☐	Simultaneous and redundantly threaded processor branch outcome queue	712/239

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18	US 20010 03230 9 A1	☐	Static branch prediction mechanism for conditional branch instructions	712/239
19	US 66979 37 B1	☐	Split history tables for branch prediction	712/240
20	US 65981 54 B1	☐	Precoding branch instructions to reduce branch-penalty in pipelined processors	712/237
21	US 65981 52 B1	☐	Increasing the overall prediction accuracy for multi-cycle branch prediction and apparatus by enabling quick recovery	712/228
22	US 65713 31 B2	☐	Static branch prediction mechanism for conditional branch instructions	712/239
23	US 65464 81 B1	☐	Split history tables for branch prediction	712/240
24	US 65300 16 B1	☐	Predicted return address selection upon matching target in branch history table with entries in return address stack	712/237
25	US 65265 02 B1	☐	Apparatus and method for speculatively updating global branch history with branch prediction prior to resolution of branch outcome	712/239
26	US 64991 01 B1	☐	Static branch prediction mechanism for conditional branch instructions	712/239
27	US 64876 37 B1	☐	Method and system for clearing dependent speculations from a request queue	711/133
28	US 64386 82 B1	☐	Method and apparatus for predicting loop exit branches	712/241
29	US 64386 56 B1	☐	Method and system for cancelling speculative cache prefetch requests	711/137
30	US 64217 74 B1	☐	Static branch predictor using opcode of instruction preceding conditional branch	712/239
31	US 64185 16 B1	☐	Method and system for managing speculative requests in a multi-level memory hierarchy	711/138
32	US 63816 91 B1	☐	Method and apparatus for reordering memory operations along multiple execution paths in a processor	712/236
33	US 63670 01 B1	☐	Processor including efficient fetch mechanism for L0 and L1 caches	712/205
34	US 63473 69 B1	☐	Method and circuit for single cycle multiple branch history table access	712/240
35	US 63381 36 B1	☐	Pairing of load-ALU-store with conditional branch	712/221
36	US 62726 24 B1	☐	Method and apparatus for predicting multiple conditional branches	712/239
37	US 62694 36 B1	☐	Superscalar microprocessor configured to predict return addresses from a return stack storage	712/23
38	US 62634 27 B1	☐	Branch prediction mechanism	712/236
39	US 62601 38 B1	☐	Method and apparatus for branch instruction processing in a processor	712/239

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40	US 6256728 B1	☐	Processor configured to selectively cancel instructions from its pipeline responsive to a predicted-taken short forward branch instruction	712/236
41	US 6247124 B1	☐	Branch prediction entry with target line index calculated using relative position of second operation of two step branch operation in a line of instructions	712/240
42	US 6247122 B1	☐	Method and apparatus for performing branch prediction combining static and dynamic branch predictors	712/239
43	US 6247097 B1	☐	Aligned instruction cache handling of instruction fetches across multiple predicted branch instructions	711/125
44	US 6233676 B1	☐	Apparatus and method for fast forward branch	712/233
45	US 6219784 B1	☐	Processor with N adders for parallel target addresses calculation	712/235
46	US 6199154 B1	☐	Selecting cache to fetch in multi-level cache system based on fetch address source and pre-fetching additional data to the cache for future access	712/205
47	US 6189091 B1	☐	Apparatus and method for speculatively updating global history and restoring same on branch misprediction detection	712/240
48	US 6167510 A	☐	Instruction cache configured to provide instructions to a microprocessor having a clock cycle time less than a cache access time of said instruction cache	712/239
49	US 6112293 A	☐	Processor configured to generate lookahead results from operand collapse unit and for inhibiting receipt/execution of the first instruction based on the lookahead result	712/216
50	US 6108775 A	☐	Dynamically loadable pattern history tables in a multi-task microprocessor	712/240
51	US 6101590 A	☐	Virtual memory system with local and global virtual address translation	711/203
52	US 6101577 A	☐	Pipelined instruction cache and branch prediction mechanism therefor	711/125
53	US 6098167 A	☐	Apparatus and method for fast unified interrupt recovery and branch recovery in processors supporting out-of-order execution	712/218
54	US 6088793 A	☐	Method and apparatus for branch execution on a multiple-instruction-set-architecture microprocessor	712/239
55	US 6065115 A	☐	Processor and method for speculatively executing instructions from multiple instruction streams indicated by a branch instruction	712/235
56	US 6044459 A	☐	Branch prediction apparatus having branch target buffer for effectively processing branch instruction	712/237
57	US 6029228 A	☐	Data prefetching of a load target buffer for post-branch instructions based on past prediction accuracy's of branch predictions	711/137
58	US 6016545 A	☐	Reduced size storage apparatus for storing cache-line-related data in a high frequency microprocessor	712/238
59	US 6014734 A	☐	Superscalar microprocessor configured to predict return addresses from a return stack storage	712/23
60	US 6003128 A	☐	Number of pipeline stages and loop length related counter differential based end-loop prediction	712/241
61	US 5983335 A	☐	Computer system having organization for multiple condition code setting and for testing instruction out-of-order	712/23
62	US 5978907 A	☐	Delayed update register for an array	712/239

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63	US 5956495 A	☐	Method and system for processing branch instructions during emulation in a data processing system	703/26
64	US 5954815 A	☐	Invalidating instructions in fetched instruction blocks upon predicted two-step branch operations with second operation relative target address	712/237
65	US 5951679 A	☐	Microprocessor circuits, systems, and methods for issuing successive iterations of a short backward branch loop in a single cycle	712/241
66	US 5943494 A	☐	Method and system for processing multiple branch instructions that write to count and link registers	712/238
67	US 5935241 A	☐	Multiple global pattern history tables for branch prediction in a microprocessor	712/240
68	US 5931944 A	☐	Branch instruction handling in a self-timed marking system	712/239
69	US 5928358 A	☐	Information processing apparatus which accurately predicts whether a branch is taken for a conditional branch instruction, using small-scale hardware	712/239
70	US 5918045 A	☐	Data processor and data processing system	712/237
71	US 5898866 A	☐	Method and apparatus for counting remaining loop instructions and pipelining the next instruction	712/241
72	US 5892936 A	☐	Speculative register file for storing speculative register states and removing dependencies between instructions utilizing the register	712/216
73	US 5881308 A	☐	Computer organization for multiple and out-of-order execution of condition code testing and setting instructions out-of-order	712/23
74	US 5878278 A	☐	Return address prediction system which adjusts the contents of return stack storage to enable continued prediction after a mispredicted branch	712/242
75	US 5875355 A	☐	Update unit for providing a delayed update to a branch prediction array	712/240
76	US 5875324 A	☐	Superscalar microprocessor which delays update of branch prediction information in response to branch misprediction until a subsequent idle clock	712/238
77	US 5870575 A	☐	Indirect unconditional branches in data processing system emulation mode	712/209
78	US 5864707 A	☐	Superscalar microprocessor configured to predict return addresses from a return stack storage	712/23
79	US 5864697 A	☐	Microprocessor using combined actual and speculative branch history prediction	712/240
80	US 5860017 A	☐	Processor and method for speculatively executing instructions from multiple instruction streams indicated by a branch instruction	712/23
81	US 5850542 A	☐	Microprocessor instruction hedge-fetching in a multiprediction branch environment	712/235
82	US 5848269 A	☐	Branch predicting mechanism for enhancing accuracy in branch prediction by reference to data	712/239
83	US 5848268 A	☐	Data processor with branch target address generating unit	712/233
84	US 5838944 A	☐	System for storing processor register data after a mispredicted branch	712/218
85	US 5835967 A	☐	Adjusting prefetch size based on source of prefetch address	711/213

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86	US 58359 51 A	☐	Branch processing unit with target cache read prioritization protocol for handling multiple hits	711/145
87	US 58322 59 A	☐	Apparatus for superscalar instruction pre-decoding using cached instruction lengths	712/238
88	US 58260 70 A	☐	Apparatus and method for maintaining status flags and condition codes using a renaming technique in an out of order floating point execution unit	712/222
89	US 58225 76 A	☐	Branch history table with branch pattern field	712/239
90	US 58225 74 A	☐	Functional unit with a pointer for mispredicted resolution, and a superscalar microprocessor employing the same	712/233
91	US 58093 24 A	☐	Multiple instruction dispatch system for pipelined microprocessor without branch breaks	712/23
92	US 57940 27 A	☐	Method and apparatus for managing the execution of instructons with proximate successive branches in a cache-based data processing system	712/238
93	US 57846 04 A	☐	Method and system for reduced run-time delay during conditional branch execution in pipelined processor systems utilizing selectively delayed sequential instruction purging	712/238
94	US 57846 03 A	☐	Fast handling of branch delay slots on mispredicted branches	712/234
95	US 57649 70 A	☐	Method and apparatus for supporting speculative branch and link/branch on count instructions	712/233
96	US 57649 40 A	☐	Processor and method for executing a branch instruction and an associated target instruction utilizing a single instruction fetch	712/206
97	US 57614 90 A	☐	Changing the meaning of a pre-decode bit in a cache memory depending on branch prediction mode	712/239
98	US 57522 59 A	☐	Instruction cache configured to provide instructions to a microprocessor having a clock cycle time less than a cache access time of said instruction cache	711/125
99	US 57520 14 A	☐	Automatic selection of branch prediction methodology for subsequent branch instruction based on outcome of previous branch prediction	712/240
100	US 57404 16 A	☐	Branch processing unit with a far target cache accessed by indirection from the target cache	712/238
101	US 57375 62 A	☐	CPU pipeline having queuing stage to facilitate branch instructions	712/218
102	US 57322 53 A	☐	Branch processing unit with target cache storing history for predicted taken branches and history cache storing history for predicted not-taken branches	712/239
103	US 57322 43 A	☐	Branch processing unit with target cache using low/high banking to support split prefetching	711/137
104	US 57064 91 A	☐	Branch processing unit with a return stack including repair using pointers from different pipe stages	712/234
105	US 56921 67 A	☐	Method for verifying the correct processing of pipelined instructions including branch instructions and self-modifying code in a microprocessor	712/226
106	US 56873 49 A	☐	Data processor with branch target address cache and subroutine return address cache and method of operation	711/137
107	US 56641 35 A	☐	Apparatus and method for reducing delays due to branches	712/201
108	US 56491 45 A	☐	Data processor processing a jump instruction	711/213

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109	US 5634136 A	☐	Data processor and method of controlling the same	712/237
110	US 5634103 A	☐	Method and system for minimizing branch misprediction penalties within a processor	712/235
111	US 5630157 A	☐	Computer organization for multiple and out-of-order execution of condition code testing and setting instructions	712/23
112	US 5617550 A	☐	Data processor generating jump target address of a jump instruction in parallel with decoding of the instruction	712/207
113	US 5606682 A	☐	Data processor with branch target address cache and subroutine return address cache and method of operation	711/204
114	US 5606676 A	☐	Branch prediction and resolution apparatus for a superscalar computer processor	712/239
115	US 5594884 A	☐	Cache memory system having a plurality of ports	711/125
116	US 5592679 A	☐	Apparatus and method for distributed control in a processor architecture	712/23
117	US 5592637 A	☐	Data processor processing a jump instruction	712/237
118	US 5590296 A	☐	Data processor processing a jump instruction	712/229
119	US 5553255 A	☐	Data processor with programmable levels of speculative instruction fetching and method of operation	712/235
120	US 5553254 A	☐	Instruction cache access and prefetch process controlled by a predicted instruction-path mechanism	712/207
121	US 5513330 A	☐	Apparatus for superscalar instruction predecoding using cached instruction lengths	712/204
122	US 5485587 A	☐	Data processor calculating branch target address of a branch instruction in parallel with decoding of the instruction	712/234
123	US 5479616 A	☐	Exception handling for prefetched instruction bytes using valid bits to identify instructions that will cause an exception	712/212
124	US 5453927 A	☐	Data processor for processing branch instructions	712/235
125	US 5442766 A	☐	Method and system for distributed instruction address translation in a multiscalar data processing system	711/204
126	US 5442756 A	☐	Branch prediction and resolution apparatus for a superscalar computer processor	712/238
127	US 5434985 A	☐	Simultaneous prediction of multiple branches for superscalar processing	712/240
128	US 5421020 A	☐	Counter register implementation for speculative execution of branch on count instructions	712/237
129	US 5410657 A	☐	Method and system for high speed floating point exception enabled operation in a multiscalar processor system	712/215
130	US 5404467 A	☐	CPU having pipelined instruction unit and effective address calculation unit with retained virtual address capability	712/207
131	US 5394530 A	☐	Arrangement for predicting a branch target address in the second iteration of a short loop	712/240

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132	US 5394529 A	☐	Branch prediction unit for high-performance processor	712/240
133	US 5381533 A	☐	Dynamic flow instruction cache memory organized around trace segments independent of virtual address line	712/215
134	US 5367703 A	☐	Method and system for enhanced branch history prediction accuracy in a superscalar processor system	712/23
135	US 5353421 A	☐	Multi-prediction branch prediction mechanism	712/240
136	US 5353419 A	☐	Memory-side driven anticipatory instruction transfer interface with processor-side instruction selection	712/235
137	US 5327547 A	☐	Two-level branch prediction cache	711/137
138	US 5313634 A	☐	Computer system branch prediction of subroutine returns	712/240
139	US 5297281 A	☐	Multiple sequence processor system	712/216
140	US 5283873 A	☐	Next line prediction apparatus for a pipelined computed system	712/207
141	US 5276882 A	☐	Subroutine return through branch history table	712/240
142	US 5265213 A	☐	Pipeline system for executing predicted branch target instruction in a cycle concurrently with the execution of branch instruction	712/240
143	US 5210831 A	☐	Methods and apparatus for insulating a branch prediction mechanism from data dependent branch table updates that result from variable test operand locations	712/240
144	US 5197136 A	☐	Processing system for branch instruction	712/238
145	US 5163140 A	☐	Two-level branch prediction cache	711/140
146	US 5155843 A	☐	Error transition mode for multi-processor system	714/5
147	US 5142634 A	☐	Branch prediction	712/240
148	US 5127091 A	☐	System for reducing delay in instruction execution by executing branch instructions in separate processor while dispatching subsequent instructions to primary processor	712/238
149	US 5034880 A	☐	Apparatus and method for executing a conditional branch instruction	712/234
150	US 4991080 A	☐	Pipeline processing apparatus for executing instructions in three streams, including branch stream pre-execution processor for pre-executing conditional branch instructions	712/206
151	US 4953121 A	☐	Circuitry for and method of controlling an instruction buffer in a data-processing system	712/241
152	US 4200927 A	☐	Multi-instruction stream branch processing mechanism	712/235
153	US 3940741 A	☐	Information processing device for processing instructions including branch instructions	712/238